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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/736,225	12/15/2000	Chien-Ping Huang	EM/HUANG/6315	8653

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/736,225	HUANG ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12-15-2000* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim R j ctions - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 31-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (US Pat. 5866948) in view of Ho (US Pat. 6455926).

Regarding claim 31, Murakami et al. disclose a single semiconductor package consisting of:

- An unsupported layer of a substrate/single layer interposer (1/15 in Fig. 8) linearly consisting of a plurality of resin/epoxy polymer portions (1 and 104 in Fig. 8 and 9 respectively) at selected locations, die pad portion (16 in Fig. 8) of the substrate/interposer layer formed in between and adjacent to the resin/epoxy
- polymer portions and lead/stud-contact portions (12 in Fig. 8) of the substrate/interposer layer adjacent to the resin/epoxy polymer portions

- a chip (2 in Fig. 8) being adhered to the die pad portion using a silver paste (Col. 6, line 26)
- a plurality of conductive elements/wires (7 in Fig. 8) electrically connecting the chip and lead/stud-contact portions, and
- a molded resin (11 in Fig. 8) covering the chip, conductive elements/wires and the resin/epoxy polymer, lead/stud-contact and die pad portions of the substrate/interposer layer

(Fig. 8-10; Col. 5, line 30- Col. 6, line 49).

Murakami et al. fail to teach:

a) the resin/epoxy polymer being a solder mask, and

b) the substrate/interposer layer being a single layer such that the die pad and lead portions are contiguous to the solder mask portions

a) Ho teaches using a substrate made of dielectric/insulating layer/material such as a polyimide/solder mask, photo-imageable epoxy resin, glass reinforced polymer/resin, etc. to achieve the desired dielectric and thermal expansion properties (Col. 5, line 35; Col. 3, line 27).

b) Murakami et al. teach in an embodiment of Fig. 12 and 13, the substrate/interposer layer being a single, integrally molded (15 in Fig. 12; Col. 6, line 63; Col. 7, line 40) and co-planar (see Col. 4, line 34), the substrate/interposer layer having die pad and lead portions (16 and 28 in Fig. 12) being contiguous to the resin/epoxy polymer portions (Col. 6, line 50- Col. 7, line 47).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder mask portions as taught by Ho such that use the die pad and lead portions of a single layer are contiguous to the solder mask portions in order to reduce the package dimension/size and to improve the dielectric properties in Murakami et al's package.

Regarding claim 32, Murakami et al. and Ho teach substantially the entire claimed structure as applied to claim 31, except the solder mask being made from photosensitive and insulative material selected from a group consisting of polyimide and UV-curable resins.

Ho further teaches using a substrate made of dielectric/insulating layer/material such as a polyimide/solder mask, photo-imageable/sensitive epoxy resin, and glass reinforced polymer/resin, etc. to achieve the desired dielectric and thermal expansion properties (Col. 5, line 35; Col. 3, line 27).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder mask the solder mask being made from photosensitive and insulative material selected from a group consisting of polyimide and UV-curable resins as taught by Ho so that package dimension/size can be reduced and the dielectric properties can be improved in Murakami et al's package.

Regarding claim 33, Murakami et al. and Ho teach substantially the entire claimed structure as applied to claims 31 and 32, wherein Murakami et al. further teach the die pad and lead portions being made of a material selected from a group consisting of nickel (Col. 6, line 18-20) and gold (Col. 5, line 5).

Regarding claims 34 and 35, the process for forming the solder mask and lead/die pad portions of the layer do not distinguish over Murakami et al. and Ho, because only the final product is relevant, not the process of making such as "coating or photo-processing" and "plating or sputtering" respectively. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not

the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claim 36, Murakami et al. and Ho teach substantially the entire claimed structure as applied to claim 31, wherein Murakami et al. further teach the conductive elements being made of a material such as gold (Col. 6, line 28).

Regarding claim 37, Murakami et al. and Ho teach substantially the entire claimed structure as applied to claim 31, except the die pad portion of the layer being replaced by the solder mask.

Murakami et al. further teach using the substrate layer having the die pad portion of the layer (not numerically referenced in Fig. 1; see top surface of 1 under the chip 2) being made of an insulating resin/glass reinforced epoxy resin (Col. 4, line 22; Col. 6, line 37).

Ho teaches using a substrate made of dielectric/insulating layer/material such as a polyimide/solder mask, photo-imageable/sensitive epoxy resin, and glass reinforced polymer/resin, etc. to achieve the desired dielectric and thermal expansion properties (Col. 5, line 35; Col. 3, line 27).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die pad portion of the layer being the solder

mask as taught by Ho so that package dimension/size can be reduced and the dielectric properties can be improved in Murakami et al's package.

Regarding claim 38, Murakami et al. disclose a single semiconductor package consisting of:

- an unsupported layer of a substrate/single layer interposer (1/15 in Fig. 8) linearly consisting of a plurality of resin/epoxy polymer portions (1 and 104 in Fig. 8 and 9 respectively) at selected locations, die pad portion (16 in Fig. 8) of the substrate/interposer layer formed in between and adjacent to the resin/epoxy
- polymer portions and lead/stud-contact portions (12 in Fig. 8) of the substrate/interposer layer adjacent to the resin/epoxy polymer portions
- a chip (2 in Fig. 8) being adhered to the die pad portion using a silver paste (Col. 6, line 26)
- a plurality of conductive elements/wires (7 in Fig. 8) electrically connecting the chip and lead/stud-contact portions, and
- a molded resin (11 in Fig. 8) covering the chip, conductive elements/wires and the resin/epoxy polymer, lead/stud-contact and die pad portions of the substrate/interposer layer

(Fig. 8-10; Col. 5, line 30- Col. 6, line 49).

Murakami et al. fail to teach:

a) the resin/epoxy polymer being a solder mask, and

b) the substrate/interposer layer being a single layer such that the die pad and lead portions are contiguous to the solder mask portions

a) Ho teaches using a substrate made of dielectric/insulating layer/material such as a polyimide/solder mask, photo-imageable epoxy resin, glass reinforced polymer/resin, etc. to achieve the desired dielectric and thermal expansion properties (Col. 5, line 35; Col. 3, line 27).

b) Murakami et al. teach in an embodiment of Fig. 12 and 13, the substrate/interposer layer being a single, integrally molded (15 in Fig. 12; Col. 6, line 63; Col. 7, line 40) and co-planar (see Col. 4, line 34), the substrate/interposer layer having die pad and lead portions (16 and 28 in Fig. 12) being contiguous to the resin/epoxy polymer portions (Col. 6, line 50- Col. 7, line 47).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder mask portions as taught by Ho such that use the die pad and lead portions of a single layer are contiguous to the solder mask portions in order to reduce the package dimension/size and to improve the dielectric properties in Murakami et al's package.

Regarding claim 39, Murakami et al. and Ho teach substantially the entire claimed structure as applied to claim 38, except the solder mask being made from photosensitive and insulative material selected from a group consisting of polyimide and UV-curable resins.

Ho further teaches using a substrate made of dielectric/insulating layer/material such as a polyimide/solder mask, photo-imageable/sensitive epoxy resin, and glass reinforced polymer/resin, etc. to achieve the desired dielectric and thermal expansion properties (Col. 5, line 35; Col. 3, line 27).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder mask the solder mask being made from photosensitive and insulative material selected from a group consisting of polyimide and UV-curable resins as taught by Ho so that package dimension/size can be reduced and the dielectric properties can be improved in Murakami et al's package.

Regarding claim 40, Murakami et al. and Ho teach substantially the entire claimed structure as applied to claims 38, wherein Murakami et al. teach the die pad and lead portions being made of a material selected from a group consisting of nickel (Col. 6, lines 18-20) and gold (Col. 5, line 5).

Regarding claims 41 and 42, the process for forming the solder mask and lead/die pad portions of the layer do not distinguish over Murakami et al. and Ho, because only the final product is relevant, not the process of making such as "coating or photo-processing" and "plating or sputtering" respectively. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claim 43, Murakami et al. and Ho teach substantially the entire claimed structure as applied to claims 38, wherein Murakami et al. further teach the conductive elements being made of a material such as gold (Col. 6, line 28).

Regarding claim 44, Murakami et al. and Ho teach substantially the entire claimed structure as applied to claims 38, except the die pad portion of the layer being replaced by the solder mask.

Murakami et al. further teach using the substrate layer having the die pad portion of the layer (not numerically referenced in Fig. 1; see top surface of 1 under the chip 2) being made of an insulating resin/glass reinforced epoxy resin (Col. 4, line 22; Col. 6, line 37).

Ho teaches using a substrate made of dielectric/insulating layer/material such as a polyimide/solder mask, photo-imageable/sensitive epoxy resin, and glass reinforced polymer/resin, etc. to achieve the desired dielectric and thermal expansion properties (Col. 5, line 35; Col. 3, line 27).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die pad portion of the layer being the solder Mask as taught by Ho so that package dimension/size can be reduced and the dielectric properties can be improved in Murakami et al's package.

Regarding claim 45, Murakami et al. and Ho teach substantially the entire claimed structure as applied to claim 31, wherein Murakami et al. further teach the top side of the substrate/single layer interposer (15 in Fig. 13; Col. 4, line 34; Col. 6, lines 60-67) being coplanar.

Regarding claim 46, Murakami et al. and Ho teach substantially the entire claimed structure as applied to claim 38, wherein Murakami et al. further teach the top side of the substrate/single layer interposer (15 in Fig. 13; Col. 4, line 34; Col. 6, lines 60-67) being coplanar.

Response to Arguments

3. Applicant's arguments filed on 07-23-03 have been fully considered but they are not persuasive.

A. Applicant contends that Murakami et al. teach using the studs and they are different than the leads or the lead layer.

However, Murakami et al. teach using the substrate comprising the studs having the bonding pad for the electrical connection of the bonding wire and the land for an external connection (13 and 14 respectively in Fig. 8), the studs further having the protruded or the coplanar configuration with respect to the substrate surface (Col. 4, lines 28-38). Furthermore, the studs in Murakami et al's substrate/package the function of conventional connection leads/lead layer on the substrate.

B. Applicant contends that the manufacturing processes are different between the invention and Murakami et al's patent since the method in the invention is characterized by using an interim substrate.

However, the claims 31-46 are directed to the device/structure and not the method of making the device and the Figures 1 and 8 in Murakami et al. showing the final structures are applied to the above claim rejections.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP

10-10-03

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800